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30GF-9118 5/14/02
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gareis, et al. : Art Unit: 2182

Serial No.: 09/682,060 : Examiner: Not yet assigned

Filed: July 16, 2001 :

For: METHOD AND SYSTEM FOR
CONFIGURING
INPUT/OUTPUT POINTS :

RECEIVED
MAY 14 2002

Technology Center 2100

PRELIMINARY AMENDMENT

Hon. Commissioner for Patents
Washington, D.C. 20231

Prior to the examination of this Application, please amend the Application as follows:

IN THE CLAIMS:

Please cancel Claims 1, 6, 12, 18, and 23.

Sgt 10/01
~~2. (once amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising at least one port controlling a configuration of the at least one pin, said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.~~

A
~~3. (once amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising:~~

~~- at least one port controlling a configuration of the at least one pin; and~~

~~at least one switch assembly comprising a solid state switch, said at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state.~~